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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,840	02/20/2004	Gururaj Nagendra	INTEL/18500	7501

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EXAMINER	
FATEHI, PARHAM R	
ART UNIT	PAPER NUMBER
2194	

MAIL DATE	DELIVERY MODE
08/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,840	NAGENDRA ET AL.	
	Examiner	Art Unit	
	Parham (Paul) R. Fatehi	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/13/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☒ Claim(s) *27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20050228, 20051003,20060913*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are pending in this application.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 2/28/2005, 10/3/2005 and 9/13/2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Objections

3. Claim 27 is objected to because of the following informalities: claim 27, ln 2 recites "application interface program" and should be changed to "application program interface". Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 5-10, 12-18, 20-22 & 25-27 are rejected under 35 U.S.C. 102(e) as being anticipated by D'Inverno et Al (EP 1 313 012) [hereafter D'Inverno]. D'Inverno was cited by Applicant in IDS filed 10/3/2005.

6. As per claims 1, 8 & 16, D'Inverno discloses generating a processor instruction proxy stub (pg 2, ln 29-31, application or part of application) associated with one or more processor instructions (pg 2, ln 1-2, code generation for target processors); and generating an optimized managed application program interface based on the processor instruction proxy stub to enable one or more features of a processor associated with the one or more processor instructions (pg 2, ln 41-49, dynamically loading onto embedded processing systems and optimizing API based on generated code that enable features of embedded processors).

7. As per claim 2, 9, 21 & 25, D'Inverno discloses generating the processor instruction proxy stub associated with the one or more processor instructions comprises generating the processor instruction proxy stub at a layer associated with a virtual machine of a managed runtime environment (pg 2, ln 55-58, generating processor instruction proxy stub at a layer associated with a virtual machine of, pg 3, ln 1-5, managed runtime environment).

8. As per claim 3, 10 & 26, D'Inverno discloses generating the processor instruction proxy stub during installation of a managed runtime application (pg 3, ln 1-3, generating instruction during installation of, pg 4, ln 50-54, runtime application).

9. As per claim 5 & 12 D'Inverno discloses generating the processor instruction proxy stub via marshaling language code of a virtual machine (pg 11, ln 10-16, marshaling language code of virtual machine).

10. As per claim 6, 13 & 18, D'Inverno discloses generating the processor instruction proxy stub in response to identifying the processor associated with the one or more processor instructions (pg 12, ln 19-20, identifying processor associated with processor instructions, and pg 2, ln 2-3, target processor).

11. As per claim 7, 14, 22 & 27, D'Inverno discloses enabling a feature associated with the one or more processor instructions during execution of a managed runtime application based on the optimized managed application program interface (pg 2, ln 51-58, exploitation of processor to enable featuring during application launch).

12. As per claim 15, D'Inverno discloses the machine accessible medium comprises one of a programmable gate array, application specific integrated circuit, erasable programmable read only memory, read only memory, random access memory, magnetic media, and optical media (pg 3, ln 38-45, random access memory).

13. As per claim 17, D'Inverno discloses the processor instruction proxy stub generator is integrated into one of a virtual machine and the compiler (pg 2, ln 2-3, virtual machine, and pg 3, ln 29-31, compiler).

14. As per claim 20, D'Inverno discloses the compiler comprises a just-in-time compiler (pg 3, ln 29-31, JIT compiler).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 4, 11, 19 & 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over D'Inverno.

17. As per claims 4, 11, 19 & 24, D'Inverno discloses generating the processor instruction proxy stub associated with one of a Streaming SIMD Extension instruction, an SSE2 instruction, and a MultiMedia Extension instruction (pg 10, ln 50-51, processing unit instruction sets).

18. D'Inverno does not explicitly disclose SSE, SSE2 and MMX. Moreover, SSE, SSE2 and MMX are commonly known in the art as common forms of processor instruction sets. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine SSE, SSE2 and MMX to the teachings of D'Inverno in order to optimize an API performance for different kinds of processors utilizing various instruction sets and thereby reaching a larger audience of users.

19. As per claim 23, D'Inverno discloses to generate a processor instruction proxy stub associated with one or more processor instructions, and to generate an optimized managed application program interface based on the processor instruction proxy stub to enable one or more features of the processor associated with the one or more processor instructions (pg 2, ln 41-49, dynamically loading onto embedded processing systems and optimizing API based on generated code that enable features of embedded processors).

20. D'Inverno does not explicitly disclose a dynamic random memory (DRAM) to store one or more optimized managed application program interfaces or a processor coupled to the DRAM. Moreover, DRAM is commonly known in the art as a type of volatile memory with structural simplicity that enables it to achieve very high densities. One of ordinary skill in the art at the time the invention was made would have modified the teachings of D'Inverno to include DRAM as a type of memory in order to achieve very high densities of memory.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Parham (Paul) R. Fatehi whose telephone number is 571-270-1407. The examiner can normally be reached on M-Th 9:30AM-8PM EST, off Fridays.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Thomson can be reached on (571)272-3718. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Fatehi
AU 2194

July 31, 2007

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

THOMSON
TENT EXAMINER